A new kind of view for a Double oven Crystal Oscillator.

Lefebvre Frederic, Weber Patrick. Dr Aubry Jean Pierre,
Oscilloquartz S.A., Neuchâtel, Switzerland.
weber@oscilloquartz.com; lefebvre@oscilloquartz.com;

New demands for minimizing space and increasing frequency stability bring us to consider a new approach on double oven Oscillators. Main application of high performance oscillators are in "GNSS disciplined" applications. To allow the assembly on a board of 4TE width, the height of the OCXO is limited to 19mm.

A major requirement is in the micro second range at 1 day holdover. Ageing and thermally induced frequency drift are to be compensated. The frequency stability <6.10^{-10} in a wide temperature range -20°c to + 70°C as well as a waterproof ness to minimize the influences of humidity. The reproducibility of the frequency change must be as low as possible in the several repetitive thermal gradients to minimize the frequency hysteresis effect.

The demand of synchronization networks for a daily frequency drift of <1.10^{-10} / day in holdover mode ask for the construction of a new mechanical-thermal structure to house the SCp3 10 MHz resonator.

Various oscillator diagrams have been compared (such as Clapp and Hartley-Colpitts) by simulation. The Clapp diagram is considered as being easier for adjustment, and needing fewer components.

Design and simulation of thermal structure will be described. In order to decrease the total height of the internal structure to <11mm, the traditional internal oven is replaced by a quartz plated on one side of the specific board that **represents** the mass of thermal inertia. All oscillator components and crystals are heated from the other side of this board by a proportional integrated thermostat.

This board becomes an "inner ovenised oscillator" and is integrated in an outer temperature stabilized structure. This structure is hermetically sealed to minimize variation induced by humidity variation that interacts as a capacity effect.

This second structure is thermally controlled by another proportional integrated thermostat.

Thermal and mechanical designs are described in details and main results (ageing, thermal drift, thermal hysteresis ...) as long as holdover performances are provided.

- **Introduction**

Oscillators are the key device of access media for modern communication systems (3G, WiMax) base station system.

Mobility requires TDD between Base stations to allow « hand over ». Then the most stringent requirement at base station level is the timing accuracy (typically nanosecond range) while the frequency requirement is not that stringent (typ. Parts in 10^{-8}).

So far, wireless transport network are based either on synchronous network (SDH, SONET) or asynchronous system, such as IP. In the first case it is possible to extract synchronisation signal from the network. Then the local requirement is just a retiming device, where the local oscillator is used as a « noise filter » and is supposed to provide hold over in case of lack of input sync. When the transport media is not synchronised (IP based, satellite back haul...) the synchronisation must be provided locally.

So far the local synchronisation options are limited to GPS or based on local time and frequency dissemination (CDMA, national radio long wave (Prang in Switzerland),). Alternative GNSS systems are under deployment, GLONASS and sooner or later, Galileo

Most promising, from cost point of view, is PTP based synchronisation (see article by A. VAllat in this conference). (2)

In all of these systems the local oscillator is the key to provide adequate stability, noise rejection and hold over capability.

The key characteristics are timing accuracy around +/- 50 ns when locked to a reference, and less than 5 to 10 micro second – first day – timing holdover.

Design critically is either on the intrinsic noise, the noise rejection capability (i.e. time constant in the control of the local OCXO on the reference signal) and on the holdover performance witch requires high intrinsic performance on ageing and thermal stability, but more stringent, capability of the ATD^{2}C process (Ageing and Thermal Drift Dynamic Compensation), which is a dynamic software tool to minimise ageing and thermal drift effect under external temperature variation during hold over.

Because of the target market price of such devices, the sole option is a concept based on simple GPS and OCXO. The performance requirement let some people to call it « ***the poor man Rubidium*** » (1).

1-4244-0647-1/07/$20.00 ©2007 IEEE

- System requirements

GPS, GPS-GLONASS are actual tool to provide timing dissemination, pps and TOD towards base station (WiMax, 3G, 4G) at the required level of performance, +/- 50 ns range, from which the reference frequency can be extracted.
Hold over mode is requested by failure in the timing transmission, either from satellite visibility problem, propagation or antenna or GPS receiver failure. Micro seconds per day of hold over is the typical requested performance.

GPS-OEM boards modules such as the following

are able to provide the suitable performance in locked mode or in hold over. +/- 50 ns locked 7 µs holdover under 15°C/H gradient in temperature range.

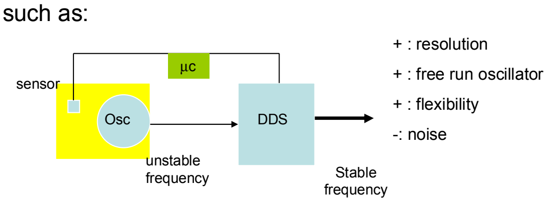
The well known timing-frequency relationship

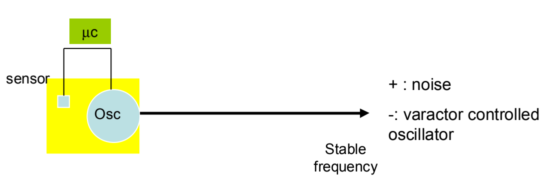
$$x(t) = x_0 + y_0\, t + \frac{D}{2}\, t^2 + \frac{\phi(t)}{2\pi \nu_0} + \int S_p(t)\, P(t)\, dt$$

Xo= initial phase offset.
Yo= initial Frequency offset.
D= daily slope, of frequency variation (ageing).
ϕ (t)= noise: white phase (WPM): Sϕ (fm) # f_m^0
1/f phase (flicker) (FPM)
White frequency (WFM)
1/f frequency (FFM)
Random walk frequency (RFM)
Sp (t) & P (t) =Sensibility to deterministic frequency perturbation and time spectrum density.

brings the link between timing accuracy and frequency deviation generated by ageing, noise and thermal sensitivity.

ATD^{2}C is required to provide the ultimate timing performance. It can be based on various configurations, such as:

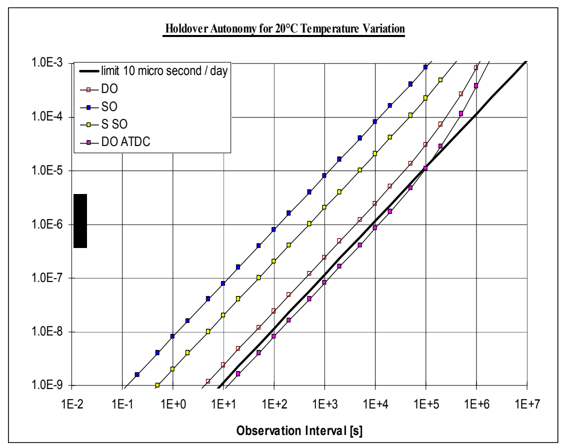




ATDC based on « post processing », such as a DDS control is probably suitable for ultimate accuracy, but suffers from poor noise characteristic, while the « pre-processing » allows low noise characteristics.
Various simulations can be derived to qualify the timing hold over capability. The following table compares hold over performance between various oscillators. Single oven using HC46 or HC37 resonators, SSO (Super single oven) and DO (double oven) using HC40 or HC 36 crystal resonators. One has included a simulation of the hold over performance achievable by a DO oscillators working in an ATDC system. From our experience, a compression (reduction) of ageing sensitivity or thermal sensitivity in a ratio of three is achievable, on a reproducible basis

	SO	S-SO	DO	DO ATDC
Therm. sens 0-70°C	2.10^{-8}	5.10^{-9}	6.10^{-10}	3.10^{-10}
ageing	2.10^{-10}	2.10^{-10}	1.10^{-10}	5.10^{-11}

The computation of eq.1 with the above parameters provides the following graph. The assumption is a 20°C temperature step @ To, entry in hold over.



The linear behaviour observed with graph of single oven and super single oven shows that the temperature induced drift is the main part of holdover drift, while the curvature observed with DO and DO-ATDC at time close to 1 day, just shows the contribution of ageing, which becomes the main timing error after one day.
It is obvious that under such « operational » conditions, i.e. in real world with real temperature gradient to be supported while in Holdover, Double oven, and even ATDC is a must to provide the required timing accuracy.

- <u>Oscillator requirement</u>

From the preceding, we can now derive the technical requirements of a proper oscillator, suitable for use in a clock device to feed up access media such as 3G, WiMax base station or synchronisation supply unit:
Size is critical: 19mm thickness is a max to equip 4TE slot cards in equipment shelf.
Critical Performances:
- ageing < 1.10^{-10} /day
- Thermal sensitivity: 6 10^{-10} in 0-70 °C

Moreover the ATDC operation requires:

- low thermal hysteresis (less than 6.10^{-11}) under thermal gradient up to 15°C per hour in the full thermal range

- <u>Oscillator design: electronics</u>

Various schemes have been compared by simulation, using Agilent EESoft EDA (ADS)
First we have compared the variation of Xtal-power under Vcc variation, Xtal-power under varactor variation, frequency variation under Vcc variation, to derive the phase loop variation under temperature variation coming from the temperature sensitivity of components. Table 1 compares Clapp and Hartley configuration without resonator.

PARAMETRE de SENSIBILITE	VALEUR	OSCILLATEUR en REFLEXION (CLAPP)		OSCILLATEUR en TRANSMISSION (HARTLEY-COLPITTS)
Variation de puissance Quartz / tension d'alim	8 --> 9V	26uW / V		28uW / V
Variation de puissance Quartz / valeur varicap	24.5pF-->25.5pF	1.88uW / pF		0.34uW / pF
Variation de Fréquence / Tension d'alim (hors défaut d'isochronisme)	8 --> 9V	1.55E-8 / V		1.1 E- 8 / V
Variation relative de puissance Quartz / shift Varicap	dPQ/PQ (Vco:0-->8V) 14pF-->67pF	66uW / 71.74uW (92%)		12.8uW / 71.2uW (18%)
Sensibilité à la Température Boucle (composants actifs seuls) Fréquence + puissance	80°C-->90°C	2E-11 / °C		9E-11 /°C
		0.1 uW / °C		0.158 uW / °C
Shift théorique / Valeur Varicap (hors défaut d'isochronisme)	14pF-->67pF (Vco:0-->8V)	3.86 E- 6		3.98 E- 6

Then we have introduced parameters regarding resonators, such anisochronism of two potential resonators, HC46 (blank size # 10mm) and HC 36 (blank size # 15mm). HC 35 is preferred because of a better ageing, low C1 and lower anisochronism (lower curvature, higher dioptres).

The comparison results are given on the next table:

DEFAUT D'ISOCHRONISME	CLAPP		HARTLEY / COLPITTS	
	HC46	HC36	HC46	HC36
/ V alim (volts)	2.34E-08	1.64E-08	2.52E-08	1.76E-08
/ C varicap (par pF)	1.69E-09	1.18E-09	3.06E-10	2.14E-10
/ Vco (V)	7.43E-09	5.20E-09	1.44E-09	1.01E-09
/ Temperature (°C)	9.00E-11	6.30E-11	1.42E-10	9.95E-11

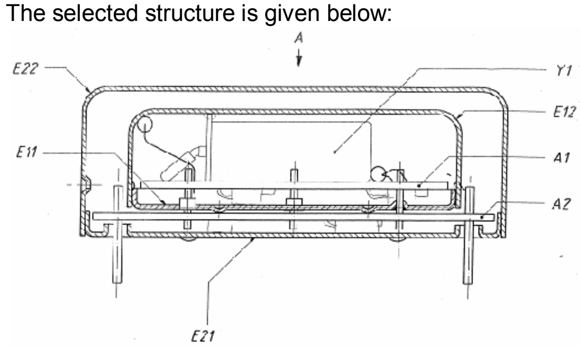
The Clapp / HC 36 have been selected, and the size of the resonator will add an additional constrain. (3).

- <u>Oscillator design: Thermo mechanical structure.</u>

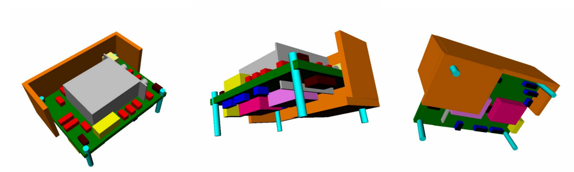
Because of the high thermal performance requested (static sensitivity < 6.10^{-10} in -20, 70°C), low thermal hysteresis (less than 6.10^{-11}) we have selected a double oven structure.
Because of the allowed thickness, and the HC36 crystal package selected, we had to simplify the double structure because there is no room for a classical DO.
Because of the low thermal hysteresis target, we have selected to operate under a hermetically sealed internal package, to prevent any influence of humidity effect under temperature variation.
From the Boyle-Mariote and Gay-Lussac laws,

$$\frac{P.V}{T} = cste$$

P=pressure, V=Volume, T=Temperature
Pressure can vary under temperature variation when in « open » air. In sealed package, moreover because this package in maintain at stable temperature, all parameters are stable and there is no longer humidity exchange between hot and cold area within the system.
Then hermetically sealed package prevent all and any frequency shifts induced by humidity variation, through variation of parasitic capacitance for example.
The selected structure is given below:



The crystal Y is mounted on a copper plate A1 which is the inner oven. This assembly is mounted in a hermetically sealed package E12 which is the outer oven. All is mounted within the 19 mm thick external package.
Thermal fitting drawings are given below:

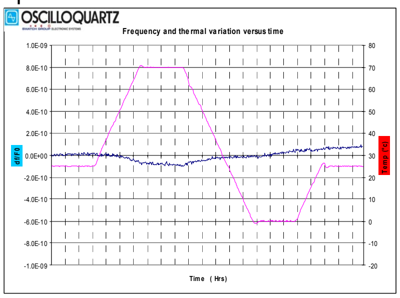


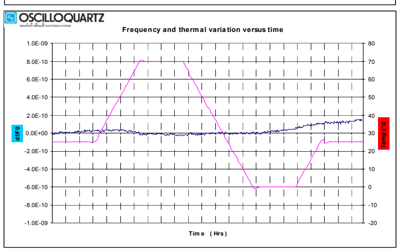
Critical issues in the adjustment process are:

- initial frequency adjustment and frequency pulling adjustment,
- hermitically of the inner can
- Reference offset between the two thermal loops and thermal adjustment.

- Oscillator performance results

The following graphs provide typical results obtained from a prototype batch.
Typical thermal performances are shown on the following graphs.
Temperature range is -20, 70°C, and the thermal gradient is # 25°C/hr, the thermal cycle is depicted also on the graph





Those samples, as the rest of the batch, are all within +/- 2.10^{-10} within -20, +70°C, which is an excellent result.
The ATD2C process /fig 2) mean to have a thermal sensor close to the oscillator providing thermal data, and providing:

- a thermal transfer function close to unity between the oscillator and the sensor,
- thermal time constant similar at the oscillator level and sensor level
- no hysteresis in the frequency-sensor curve under temperature cycle, i.e. a minimum frequency offset in frequency at the same temperature when temperature gradient is positive or negative,

It is possible to implement software determining the frequency deviation to apply and compensate the thermal drift.
This data twill is initial data, and the thermal characteristic must be reproducible with time.
Theoretically it must be possible to compensate any oscillator. The real fact is that very high intrinsic performance is required. The expected « compression » ratio is not higher than 3 to 5, to take into account components ageing drift generated.

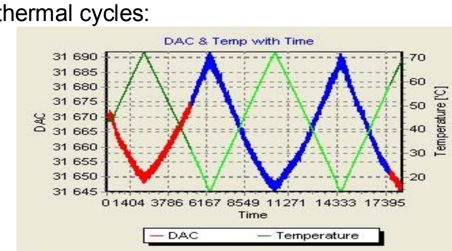
On a similar way, when thermal effect are removed, it is possible to dynamically record the ageing of the oscillator (while in locked mode under normal operation) and then to use the last set of ageing data from the holdover behaviour.

In order to select low thermal hysteresis oscillator, each oscillator is submitted to a thermal cycle (2 or 3 cycles). Frequency vs. temperature and sensor versus temperature are simultaneously recorded.

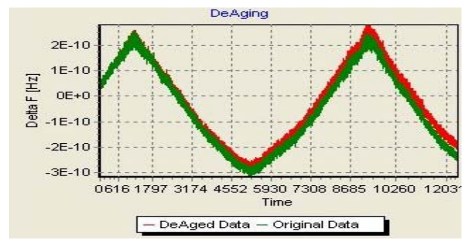
Then we can determine the hysteresis offset on the frequency-sensor curve on 2-3 cycles.
Selection is made on the criteria offset < 8 10^{-11} in 70% of the measured point of the thermal hysteresis cycle. Interpolation is made by software.

The following graphs describe this measurement:

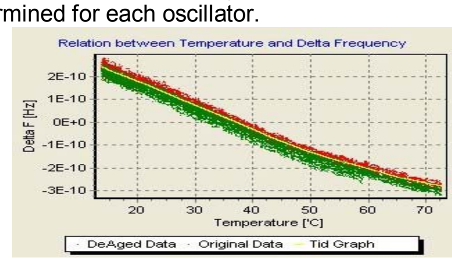
The frequency (here the DAC value towards nominal frequency) and temperature are recorded during 2 and half thermal cycles:



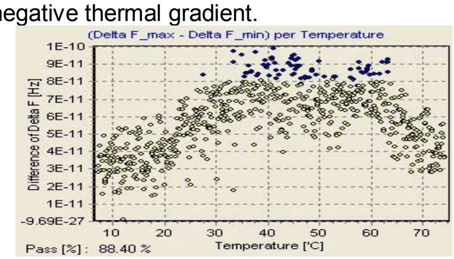
The following graph provides the « de-aged » curve, when the average ageing is removed from individual data:



Then the final « frequency – sensor » map is finally determined for each oscillator.

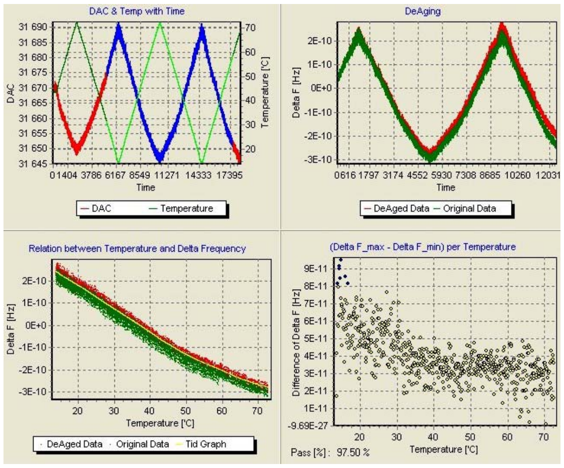


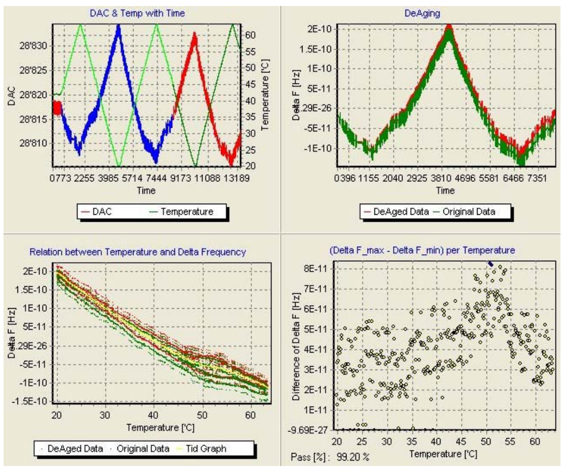
The next curve provides the frequency offset between frequencies measured during positive thermal gradient and negative thermal gradient.



Offset is lower than 8.10^{-11} in more than 70% of calculated points, which is by far enough to interpolate and gain a ratio greater than three in the frequency-temperature characteristic.

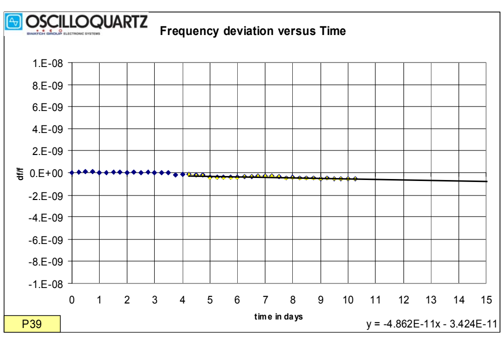
- Over Samples:

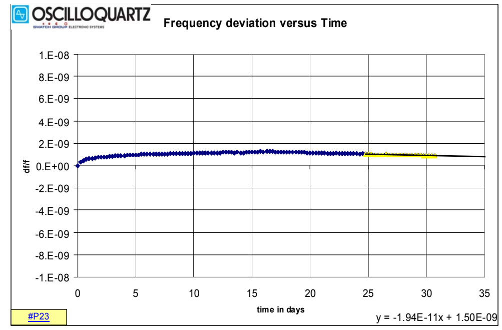




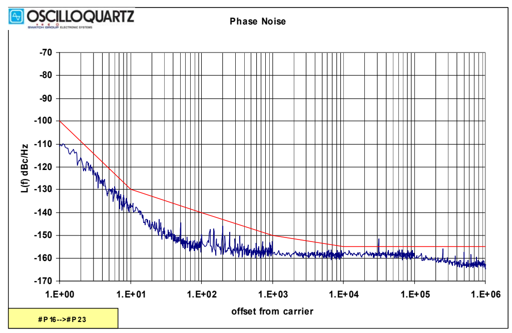
- Oscillator performance

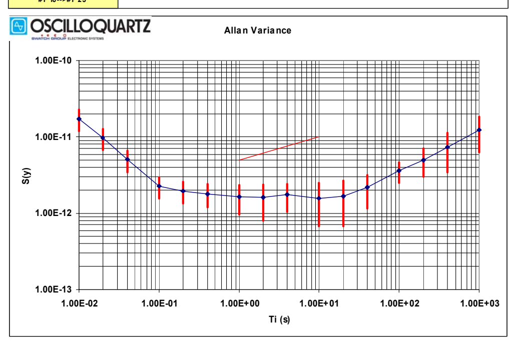
This oscillator exhibits following performances.
Ageing is less than 1.10^{-10} per day, without specific pre-ageing,



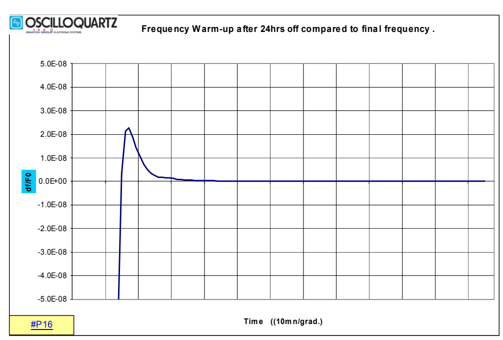


Short term stability and phase noise are given below. As expected from the oscillator design and resonator selected, Allan variance lower than 2.10^{-12} is measured up to 30s integrations time, and the most remarkable point of the phase noise is the measured data lower than -100 dBc/Hz @ 1 Hz from the carrier (Fo is 10 MHz). Noise floor is around: -160 dBc/Hz.





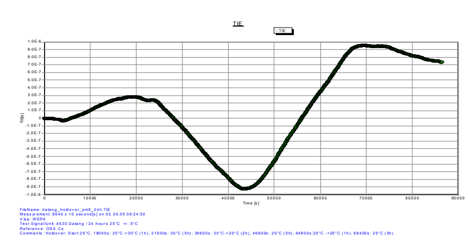
Last but not least, the warm up results show low overshoot and a warm up time lower than 15 minutes to be within +/-5.10^{-8} of final frequency, and 25 minutes to be within +/-2.10^{-9} of final frequency.

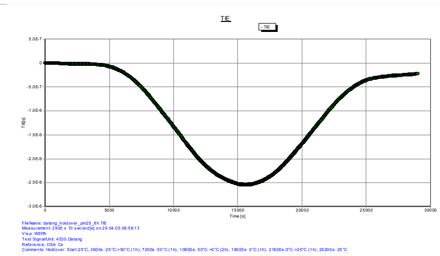


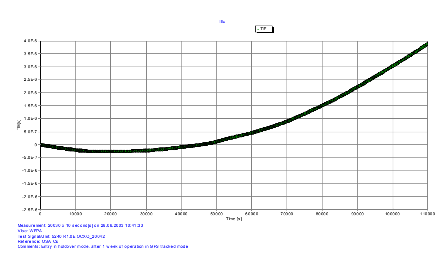
- Holdover Characteristic

As mentioned in the introduction, the main purpose of such an oscillator is to be integrated in a GPS receiver - or GNSS or PTP-client, to be used as a time reference in 3G, WiMax or similar base station. The main characteristic is to provide a high stable oscillator to allow high noise rejection capability, and to provide micro-second / 1 day holdover capability under normal operational condition.
The measured performance is then the following:
The first graph is the holdover performance, under high temperature variation (+/- 5 and +/- 25 °C around 25 °C) of a GNSS receiver equipped with a low profile 19mm OCXO (5.10^{-10} frequency deviation in temperature range).

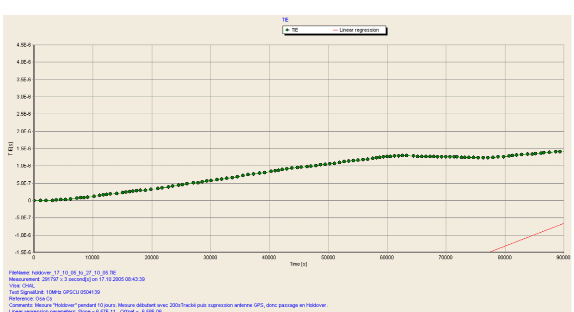
24 hours, 25°C +/-5°C







The last curve gives the holdover performance of a GNSS receiver equipped with high performance low profile and under ATDC. (4).



- Conclusion

In this paper we have describe the « why and how » of the design of a low profile 19mm double oven OCXO. The design is also suitable to operate under ATDC, Ageing and Thermal Dynamic Drift Compensation, in order to partially compensate the thermal and ageing natural drift when entering in Hold over performance.

Beside the intrinsic frequency-temperature stability (less than 5.10^{-10} in -20, 70°C), a major achievement is the micro second range at 1 day holdover capability.
Ageing and thermally induced frequency drift are compensated via ATD^2C. Hermetically sealed inner package is used to minimize the influences of humidity, to enter ATD2C mode.
Various oscillator diagrams have been compared (such as Clapp and Hartley-Colpitts) by simulation. The Clapp scheme has been selected.

Despite the size of the selected resonator (the SCp3 10 MHz HC36), the overall height is less than 19mm. Design and simulation of thermal structure has been described. The internal oven structure, (less than 11 mm), is a copper plate receiving the quartz resonator on one side. All oscillator components and crystal are heated from the other side of this board

This board becomes the "inner ovenised oscillator" and is integrated in an outer temperature stabilized structure. This structure is hermetically sealed to minimize variation induced by humidity variation that interacts as a capacity effect.

This second structure is thermally controlled by the outer oven.

Main results (ageing, thermal drift, thermal hysteresis ...) as long as holdover performances achieved by this design made it suitable for any WiMax, 3G, 4G and other base station synchronisation, and made it at the proper cost.

References.

(1) - M Bloch, private joke From M. Aubry.
(2)-A.Valat. Oscilloquartz software development engineer
(3)- J. Chauvin. Oscilloquartz XO development engineer
(4) – P.Weber Oscilloquartz R&D Telecom department manager